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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/606,258	06/24/2003	Mun Tutt Chin	9818-082-999	4508

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EXAMINER	
SAEED, USMAAN	
ART UNIT	**PAPER NUMBER**
2166	

DATE MAILED: 03/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/606,258	CHIN ET AL.	
	Examiner	Art Unit	
	Usmaan Saeed	2166	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *22-24* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Group I, Claims 1-21, drawn to application of databases, classified in class 707, subclass 104.1.

II. Group II, Claims 22-24, drawn to testing of wafers, classified in class 716, subclass 4.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because Claims of group I are in database environment and are directed towards application of databases and Claims of group II are not in database environment and are directed towards testing of wafers.

Because these inventions are independent or distinct for the reasons given above and have acquired a separate status in the art in view of their different classification, restriction for examination purposes as indicated is proper.

Because these inventions are independent or distinct for the reasons given above and the inventions require a different field of search (see MPEP § 808.02), restriction for examination purposes as indicated is proper.

Because these inventions are independent or distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

During a telephone conversation with Mr. Morris, Francis on March 1, 2006 a provisional election was made with traverse to prosecute the invention of Group I, claim 1-21. Affirmation of this election must be made by applicant in replying to this Office action. Claim 22-24 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b)

if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-6, 8-13, and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Broberg et al.** (**Broberg** hereinafter) U.S. PG Pub No. 2004/0128641 in view of **Ryo Atsumi**. (**Atsumi** hereinafter) U.S. Patent No. 5,594,639.

With respect to claim 1, **Broberg** teaches **a method for manufacturing integrated circuits meeting customer special requirements with multiple subcontractors in remote locations, comprising the steps of:**

"receiving a customer transaction file via the internet" as the processor 30 may access one or more of the generation tools, the required data, other various applications components, programs, objects, modules, etc., resident on one or more processors in another computer coupled to computer 20 via a network 18, e.g., in a distributed or client-server computing environment whereby the processing to implement the functions of the suite or one of the tools may be allocated to multiple computers over a network (**Broberg** Paragraph 0026).

"extracting a set of customer special requirements from said transaction file" as the suite of generation tools described herein interprets an application set, also described herein, and a customer's requirements for an integrated circuit (**Broberg** Paragraph 0028).

"updating a customer rule set database with the set of customer special requirements" as the manager 732 further maintains the request order of the elements to be constructed, the physical placement detail of the customer

logic from the design database 784 (**Broberg** Paragraph 0055). Examiner interprets the design database as the customer rule set database since it contains the customer logic.

"selecting wafers in a die bank database in accordance with said customer rule set database" as the resource selector 736 to provide a list of available elements which can be used to construct the requested circuit; (d) updates the resource database 734 with the complete view of generated elements for use in further optimization passes (**Broberg** Paragraph 0055). The manager 732 further maintains the request order of the elements to be constructed, the physical placement detail of the customer logic from the design database 784 (**Broberg** Paragraph 0055). Examiner interprets the resource database as die bank database.

Broberg teaches the elements of claim 1 as noted above but does not explicitly teaches **"validating special release requirements for said selected wafers in accordance with an assembly capability database" and "issuing electronic die release orders for said wafers to a plurality of subcontractors."**

However, **Atsumi** discloses **"validating special release requirements for said selected wafers in accordance with an assembly capability database" and "issuing electronic die release orders for said wafers to a plurality of subcontractors"** as the dispatching processing unit 36 determines the schedule, lot, and operation priority, the load explosion processing unit 38 executes resources/lead time explosion and resources/loads explosion for

individual orders and the requirements planning processing unit 40 projects the loads for individual resources, and the result of these processings is output to the order load ledger 48 and further to an external release order ledger 50. An order registered to the external release order ledger 50 becomes an order to the outside i.e., a sub-order, and it becomes an output unit to a sub-contractor. Furthermore, it also functions as a report input unit for the result of a plan or the execution of the plan from the sub-order, which is registered to a progress database 46 to be described later (**Atsumi** Col 8, 63-67 & Col 9, Lines 1-9). Examiner interprets the progress database as the assembly capability database.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of the cited references because **Atsumi's** teachings would have allowed **Broberg** to provide a general-purpose order processing control module, which has an internal structure to process sequentially input actual orders and the orders are controlled while exchanging them to and from the outside.

Claims 8 and 15 are essentially the same as claim 1 except they set forth the claimed invention as a computer program and a system and are rejected for the same reasons as applied hereinabove.

With respect to claim 2, **Broberg** teaches **"the method of claim 1, further comprising the steps of:**

"retrieving wafer data from foundry subcontractors via the Internet" as the resource selector 736 to provide a list of available elements which can be used to construct the requested circuit (**Broberg** Paragraph 0055).

"retrieving die bank lot details from a shop floor management system" as the floorplan shell describes the location of the physical slice resources on the slice, particularly physical placement requirements on the transistor fabric and power grid to enable R-cell hardmac creation. The floorplan shell further has the physical placement requirements on the memories, configurable I/Os, PLL, etc. used in allocating the resources of the slice by the suite of generation tools. Thus, the shells provide proven interfaces and controllers that may be in compliance with industry standards, so the chip developer and/or the customer need only concentrate on developing their differentiating logic (**Broberg** Paragraph 0050). Examiner interprets floorplan shell as die bank lot.

"mapping said wafer data to said die bank lot" as the synthesis shell 858 and the floorplan shell 860 provide input to the static timing analysis shell 856. The documentation shell 862 is provided as output (**Broberg** Paragraph 0063). The documentation has the resource/(wafer data) of the slice, and the floorplan has the physical location of the resources and the data with the resources and the location is being linked/mapped by the timing analysis shell.

"updating said die bank database with said wafer data" as the resource selector 736 to provide a list of available elements which can be used to construct the requested circuit; (d) updates the resource database 734 with the

complete view of generated elements for use in further optimization passes (**Broberg** Paragraph 0055).

Broberg teaches the elements of claim 2 as noted above but does not explicitly teaches **"subcontractors."**

However, **Atsumi** discloses **"subcontractors"** as an order registered to the external release order ledger 50 becomes an order to the outside i.e., a sub-order, and it becomes an output unit to a sub-contractor (**Atsumi** Col 8, 63-67 & Col 9, Lines 1-9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of the cited references because **Atsumi's** teachings would have allowed **Broberg** to provide a general-purpose order processing control module, which has an internal structure to process sequentially input actual orders and the orders are controlled while exchanging them to and from the outside.

Claims 9 and 16 are essentially the same as claim 2 except they set forth the claimed invention as a computer program and a system and are rejected for the same reasons as applied hereinabove.

With respect to claim 3, **Broberg** teaches **"the method of claim 1, further comprising the steps of:**

"retrieving assembly capability data from a corporate planning system" as the resource manager 732 has selected the candidate elements,

these elements along with the customer requirement 720 are passed to the composer 738. The composer 738 generates the design views 750, i.e., the RTL, simulation array, timing constraints, synthesis scripts, for the requested design, which may be in Verilog, VHDL, or other design language selected. The composer 738 also informs the manager 732 if it is not possible to create the requested resource from the particular slice (**Broberg** Paragraph 0057). Examiner interprets the RTL, simulation array, timing constraints, synthesis scripts, for the requested design as assembly capability data.

"retrieving manufacturing document data from a document control system" as a documentation shell provides templates to interface with the suite of generation tools and may provide an interface by which the user module can be compatibly input to the suite. Typically, the documentation shell may include the resources of slice including the total I/Os and memories available, the I/Os and memories available after assignment and generation, the interface timing diagrams, and the block functional specifications (**Broberg** Paragraph 0049). Examiner interprets document shell as to include data for manufacturing.

"updating said assembly capability database" as updates the resource database 734 with the complete view of generated elements for use in further optimization passes (**Broberg** Paragraph 0055).

Broberg teaches the elements of claim 3 as noted above but does not explicitly teaches **"assembly capability database."**

However, **Atsumi** discloses **"assembly capability database"** as a report input unit for the result of a plan or the execution of the plan from the sub-order,

which is registered to a progress database 46 to be described later (**Atsumi** Col 8, 63-67 & Col 9, Lines 1-9). Examiner interprets the progress database as the assembly capability database.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of the cited references because **Atsumi's** teachings would have allowed **Broberg** to provide a general-purpose order processing control module, which has an internal structure to process sequentially input actual orders and the orders are controlled while exchanging them to and from the outside.

Claims 10 and 17 are essentially the same as claim 3 except they set forth the claimed invention as a computer program and a system and are rejected for the same reasons as applied hereinabove.

With respect to claim 4, **Broberg** teaches **"the method of claim 1, wherein selecting wafers in a die bank database further comprises the steps of:**

"identifying wafers that meet customer special requirements in accordance with information obtained from a wafer test system" as surrounding the RTL logic of the generated module 410 is the user module 420. Any customer logic provided will be inserted in the user module 420 and will be conditioned by an RTL analysis tool to implement the customer's logic quickly. An example of such an RTL analysis tool is TERAFORM, a commercially

available tool that identifies potential timing and design closure issues of the customer's specification early in the design cycle. Also included in the user module 420 are instantiated diffused and R-cell memory and their corresponding wrappers, and registers, and a list of ports having tie-offs, i.e., the list of I/O ports that will not be used. These memory, registers, and list of ports can be generated by one of the suite of generation tools or may be provided as part of the customer requirements (**Broberg** Paragraph 0042).

"tagging said wafers" as the resource selector 736 to provide a list of available elements which can be used to construct the requested circuit (**Broberg** Paragraph 0055).

"updating said die bank database" as the resource selector 736 to provide a list of available elements which can be used to construct the requested circuit; (d) updates the resource database 734 with the complete view of generated elements for use in further optimization passes (**Broberg** Paragraph 0055).

Claims 11 and 18 are essentially the same as claim 4 except they set forth the claimed invention as a computer program and a system and are rejected for the same reasons as applied hereinabove.

With respect to claim 5, **Broberg** teaches **the method of claim 1, wherein validating special release parameters comprises the steps of:**

"retrieving customer special release details from said customer rule set database" as the manager 732 further maintains the request order of the elements to be constructed, the physical placement detail of the customer logic from the design database 784 (**Broberg** Paragraph 0055). Examiner interprets the design database as the customer rule set database since it contains the customer logic.

"retrieving assembly capabilities of subcontractors from said assembly capability database" as the resource manager 732 has selected the candidate elements, these elements along with the customer requirement 720 are passed to the composer 738. The composer 738 generates the design views 750, i.e., the RTL, simulation array, timing constraints, synthesis scripts, for the requested design, which may be in Verilog, VHDL, or other design language selected. The composer 738 also informs the manager 732 if it is not possible to create the requested resource from the particular slice (**Broberg** Paragraph 0057). Examiner interprets the RTL, simulation array, timing constraints, synthesis scripts, for the requested design as assembly capability data.

Broberg teaches the elements of claim 5 as noted above but does not explicitly teaches **"release orders", "assembly capability database" and "validating said customer special release details against said assembly capabilities of subcontractors."**

However, **Atsumi** discloses **"release orders", "assembly capability database"** as the dispatching processing unit 36 determines the schedule, lot, and operation priority, the load explosion processing unit 38 executes

resources/lead time explosion and resources/loads explosion for individual orders and the requirements planning processing unit 40 projects the loads for individual resources, and the result of these processings is output to the order load ledger 48 and further to an external release order ledger 50. An order registered to the external release order ledger 50 becomes an order to the outside i.e., a sub-order, and it becomes an output unit to a sub-contractor. Furthermore, it also functions as a report input unit for the result of a plan or the execution of the plan from the sub-order, which is registered to a progress database 46 to be described later (**Atsumi** Col 8, 63-67 & Col 9, Lines 1-9). Examiner interprets the progress database as the assembly capability database. **and "validating said customer special release details against said assembly capabilities of subcontractors"** as wherein the dispatching processing unit 36 receives an order generated as a result of the explosion of orders into component requirements and determines the date of the starting point or ending point of the order, and the load explosion processing unit 38 generates a process sequence by using a process chart and explodes the load for the individual resources and inputs the same to the requirements planning processing unit 40 to plan the load for the respective resources such as equipments, manpower, tools, jigs, orders to sub-contractors, and the like (**Atsumi** Col 4, Lines 41-51).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of the cited references because **Atsumi's** teachings would have allowed **Broberg** to provide a general-purpose

order processing control module, which has an internal structure to process sequentially input actual orders and the orders are controlled while exchanging them to and from the outside.

Claims 12 and 19 are essentially the same as claim 5 except they set forth the claimed invention as a computer program and a system and are rejected for the same reasons as applied hereinabove.

With respect to claim 6, **Broberg** teaches **the method of claim 1, wherein issuing electronic die release orders to a plurality of subcontractors comprises the steps of:**

"electronic data and internet" as the processor 30 may access one or more of the generation tools, the required data, other various applications components, programs, objects, modules, etc., resident on one or more processors in another computer coupled to computer 20 via a network 18, e.g., in a distributed or client-server computing environment whereby the processing to implement the functions of the suite or one of the tools may be allocated to multiple computers over a network (**Broberg** Paragraph 0026).

Broberg teaches the elements of claim 6 as noted above but does not explicitly teaches **"generating die release order file for said selected wafers and said validated special release requirements" and "transfering said electronic die release order file to subcontractors"** as the dispatching processing unit 36 determines the schedule, lot, and operation priority, the load

explosion processing unit 38 executes resources/lead time explosion and resources/loads explosion for individual orders and the requirements planning processing unit 40 projects the loads for individual resources, and the result of these processings is output to the order load ledger 48 and further to an external release order ledger 50. An order registered to the external release order ledger 50 becomes an order to the outside i.e., a sub-order, and it becomes an output unit to a sub-contractor. Furthermore, it also functions as a report input unit for the result of a plan or the execution of the plan from the sub-order, which is registered to a progress database 46 to be described later (**Atsumi** Col 8, 63-67 & Col 9, Lines 1-9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of the cited references because **Atsumi's** teachings would have allowed **Broberg** to provide a general-purpose order processing control module, which has an internal structure to process sequentially input actual orders and the orders are controlled while exchanging them to and from the outside.

Claims 13 and 20 are essentially the same as claim 6 except they set forth the claimed invention as a computer program and a system and are rejected for the same reasons as applied hereinabove.

Claims 7, 14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Broberg et al**. (**Broberg** hereinafter) U.S. PG Pub No.

2004/0128641 in view of **Ryo Atsumi**. (**Atsumi** hereinafter) U.S. Patent No. 5,594,639 as applied to claim 1-6, 8-13, and 15-20 above further in view of **Sedra et al.** (**Sedra** hereinafter) (NPL "Microelectronic circuits" Oxford University Press 1998 Pages 354-358).

With respect to claim 7, **Broberg** teaches **"the method of claim 1, wherein said customer special requirements contain at least one parameter selected from the group consisting of n-channel breakdown voltage, n-channel saturation current, p-channel saturation current, n-channel threshold voltage, p-channel threshold voltage, yield before bake and yield after bake"** as the resource selector 736 performs a local optimization across a weighting of the parameters and builds a list of elements to support the requested design (**Broberg** Paragraph 0056).

Broberg and Atsumi teaches the elements of claim 7 as noted above but does not explicitly teaches **"group consisting of n-channel breakdown voltage, n-channel saturation current, p-channel saturation current, n-channel threshold voltage, p-channel threshold voltage, yield before bake and yield after bake."**

However, **Sedra** discloses **"group consisting of n-channel breakdown voltage, n-channel saturation current, p-channel saturation current, n-channel threshold voltage, p-channel threshold voltage, yield before bake and yield after bake"** as current is conducted by only one type carrier (electrons

or hole) depending on the type of FET (n channel or p channel) (Sedra Page 354).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teaching of the cited references because **Sedra's** teachings would have allowed **Atsumi and Broberg** to manufacture the integrated circuits according to customer's requirements in an efficient and timely manner by the use of these parameters.

Claims 14 and 21 are essentially the same as claim 7 except they set forth the claimed invention as a computer program and a system and are rejected for the same reasons as applied hereinabove.

Conclusion

The prior art made of record and not replied upon is considered pertinent to applicant's disclosure is listed on 892 form.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Usmaan Saeed whose telephone number is (571)272-4046. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hosain Alam can be reached on (571)272-3978. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Usmaan Saeed
Patent Examiner
Art Unit: 2166

Hosain Alam
Supervisor

US
February 23, 2006